Remarks

Claims 1-23 are pending in the current application. The claims have not been amended.

Allowable Subject Matter

Claims 5, 8, 13, 15, 20 and 23 are indicated as containing allowable subject matter and would be allowable if rewritten in independent form. Applicant thanks the Examiner for the indication of allowable subject matter.

Drawings

The drawings stand objected to under 37 CFR 1.83(a). The Examiner has requested that the drawings be amended to show the three stages as disclosed in Claims 7 and 8 or canceled from the claims. Claim 7 recites "wherein said compressing four pixel values and a rounding vector is performed in three stages." Claim 8 recites "wherein said three stages comprise: compressing three of said four pixel values into a second sum vector and a second carry vector; compressing the fourth pixel value, the rounding vector, and the second sum vector into a third sum vector and a third carry vector; and compressing the second carry vector, third sum vector and third carry vectors into said first sum and first carry vectors."

Applicant respectfully traverses this objection and the drawings have not been amended. FIG. 3 illustrates three stages: first CSA stage 302, second CSA stage 304 and third CSA stage 306. Paragraphs [0016] and [0017] of Applicant's specification describes these stages in detail:

> [0016] Each 5-to-2 compressor 110-113 may include three stages of "3-to-2" compressors, a first carry shift adder (CSA) stage 302, a second CSA stage 304, and a third CSA stage 306. The 3-to-2 compressors each compress three vectors into a sum vector and a carry vector. The different 5-to-2 compressors 110-113

operate similarly, but on different pixel values. Consider the 5-to-2 compressor 110, which compresses the operands wRm[byte 4], wRn[byte 4], wRm[byte 3], wRn[byte 3], and the rounding vector R. In this case, WRm<0>...<7> correspond to the bits of wRm[byte 3], WRn<0>...<7> correspond to the bits of wRn[byte 3], WRm<8>...<15> correspond to the bits of wRm[byte 4], and WRn<8>...<15> correspond to the bits of wRn[byte 4]. In the first CSA stage 302, wRm[byte 3], wRn[byte 3], and wRm[byte 4] are compressed into a sum vector S0 having bits S0<0>...S0<7> and a carry vector C0 having bits C0<0>...C0<7>. In the second stage, wRn[byte 4], S0, and a Round vector of 2_{10} ($x<1>x<0> = 10_2$) are compressed into a sum vector S1 having bits S1<0>...S1<7> and a carry vector C1 having bits C1<0>...C1<7>. In the third stage, vectors C0, S1, and C1 are compressed into a sum vector S2 having bits S2<0>...S2<7> and a carry vector having bits C2<0>...C2<7>.

[0017] As described above, the least two LSBs of the result of (wRn[byte 4] + wRm[byte 4] + wRn[byte 3] + wRm[byte 3] + Round) are discarded in the shifting operation (>>2). The only useful data from the two LSBs is the carry out C2<0>. Since the LSBs of the three input vectors C0, S1, and C1 in the third stage 304 of the operation 300 are 0, S1<0>, and 0, respectively, the carry out, C2<0>, equals 0.

35 U.S.C. 102 Rejections

Claims 1 and 16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Jiang (U.S. Pat. No. 6,078,941).

Applicant respectfully traverses these rejections because the cited references do not disclose or suggest every element of any claim, as the following analysis shows.

CLAIM 1

The Office Action dated February 17, 2005 relies on multiplier 120 of FIG. 1 of Jiang to teach "compressing a plurality of pixel values and a rounding vector into a first sum vector and a first carry vector" as recited in Claim 1. However, multiplier 120 multiples two 288-bit vectors outputting a 576 bit sum vector and a 576 carry vector.

Multiplying is not the same as compressing. Even if, as asserted by the Office Action, the IFU input provides a divide-by number, dividing is not the same as compressing.

The Office Action also states that the IFU input of Jiang can provide the rounding vector. However, the IFU input is not input to multiplier 120 of Jiang.

The Office Action also states that Jiang teaches "discarding a least significant bit of the first carry vector" and "discarding a two least significant bits of the first sum vector" as recited in Claim 1 is done by the use of the rounding value input into the multiplier. Jiang does not show a rounding value input into the multiplier.

The rejection of Claim 1 is thus unsupported, and must be withdrawn.

CLAIM 16

For similar reasons as asserted above, Jian et al. does not teach "instructions operative to cause a machine to: compress a plurality of pixel values and a rounding vector into a first sum vector and a first carry vector; discard a least significant bit of the first carry vector; and discard a two least significant bits of the first sum vector" as recited in Claim 16.

The rejection of Claim 16 is thus unsupported, and must be withdrawn.

35 U.S.C. 103 Rejections

Claims 2-4, 6-7, 9-12, 14, 17-19, and 21-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang.

Applicant respectfully traverses these rejections because the cited references do not disclose or suggest every element of any claim, as the following analysis shows.

Claim 1 is allowable as argued above. Claims 2-4 and 6-7 depend from allowable Claim 1 and are allowable for at least this reason.

Claim 16 is allowable as argued above. Claims 17-19 and 21-22 depend from allowable Claim 16 and are allowable for at least this reason.

CLAIM 9

For similar reasons as asserted above, Jian et al. does not teach "a compressor stage including a plurality of compressors, each compressor operative to compress a plurality of operands and a rounding vector into a first sum vector and a first carry vector and to discard a two least significant bits (LSBs) of said first sum vector and an LSB of the first carry vector" as recited in Claim 9.

The rejection of Claim 9 is thus unsupported, and must be withdrawn. Claims 10-12 and 14 depend from allowable Claim 9 and are allowable for at least this reason.

Conclusion

For the foregoing reasons, it is submitted that the application is in condition for allowance, and indication of allowance by the Examiner is respectfully requested. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as possible. If any fee insufficiency or overpayment is found, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

Intel Corporation

Date: May 16, 2005 /Rita M. Wisor/

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